In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Original) A method for distributed device identifier number
2   assignment and device counting in a serially connected chain of
3   devices, comprising:
4   receiving a first sequence of received pulses;
5   determining a unique device identifier based upon the first
6   sequence received of pulses;
7   transmitting a first sequence of transmitted pulses;
8   receiving a second sequence of received pulses;
9   transmitting a second sequence of transmitted pulses; and
10   determining a total device count based upon the first and
11   second sequences of received pulses.

1   2.   (Original) The method of claim 1, further comprising the step
2   of initializing a first and a second memory locations before
3   receiving the first sequence of received pulses.

1   3.   (Original) The method of claim 2, wherein the first and second
2   memory locations are both initialized to a value that is equal to a
3   maximum allowed number of devices in the serially connected chain.

1   4.   (Original) The method of claim 3, wherein the determining a
2   unique device identifier step comprises:
3   counting a number of pulses in the first sequence of received
4   pulses; and
5   subtracting the number of pulses from the value stored in the
6   first memory location.

1　5.　(Original) The method of claim 4, wherein the unique device
2　identifier is stored back to the first memory location.

1　6.　(Original) The method of claim 3, wherein the determining a
2　total device count comprises:
3　　counting the number of pulses in the second sequence of
4　received pulses;
5　　subtracting the number of pulses from the value stored in the
6　second memory location to obtain a difference; and
7　　adding the value stored in the first memory location and the
8　difference.

1　7.　(Original) The method of claim 6, further comprising
2　incrementing the result of adding the value stored in the first
3　memory location and the difference by one (1.0).

1　8.　(Original) The method of claim 1, wherein the first sequence
2　of transmitted pulses is a sequence of pulses with one pulse less
3　than the number of pulses in the first sequence of received pulses.

1　9.　(Original) The method of claim 1, wherein the second sequence
2　of transmitted pulses is a sequence of pulses with one pulse less
3　than the number of pulses in the second sequence of received
4　pulses.

1　10.　(Original) The method of claim 1, wherein the receiving first
2　received sequence and the transmitting first transmitted sequence
3　are received and transmitted over different input/output
4　connections.

1　11.　(Original) The method of claim 1, wherein the receiving second
2　received sequence and the transmitting second transmitted sequence

3   are received and transmitted over different input/output
4   connections.

1   12. (Original) The method of claim 1, wherein the receiving first
2   received sequence and transmitting second transmitted sequence are
3   received and transmitted over the same input/output connection.

1   13. (Original) The method of claim 1, wherein the transmitting
2   first transmitted sequence and receiving second received sequence
3   are received and transmitted over the same input/output connection.

1   14. (Original) A semiconductor device comprising:
2   a counter, coupled to an input/output node, the counter for
3   counting a number of pulses in a sequence of pulses received at the
4   input/output node;
5   a first storage location to store a first count result; and
6   a pulse generator, for generating a specified length sequence
7   of pulses, the specified length being one less than the number of
8   pulses in the sequence of pulses received at the input/output node.

1   15. (Original) The semiconductor device of claim 14, wherein the
2   semiconductor device uses the first count result as a device
3   identifier.

1   16. (Original) The semiconductor device of claim 14, wherein a
2   second sequence of pulses is received at a second input/output
3   node.

1   17. (Original) The semiconductor device of claim 16, further
2   comprising a second storage location to store a second count
3   result.

1 18. (Original) The semiconductor device of claim 17, wherein the
2 first and second count results are combined to provide information
3 on a total number of devices in a system that includes the
4 semiconductor device.

1 19. (Original) The semiconductor device of claim 14, further
2 comprising a controller, coupled to the first storage location, the
3 counter and the pulse generator, the controller controlling the
4 operation of the counter and the pulse generator.

1 20. (Original) The semiconductor device of claim 19, wherein the
2 controller is a microcontroller.

1 21. (Original) The semiconductor device of claim 19, wherein the
2 controller is a microprocessor.

1 22. (Original) The semiconductor device of claim 19, wherein the
2 controller is a finite state machine.

1 23. (Original) A system comprising:
2   a processor, coupled to a sequence of least one codec, adapted
3 to processing digital data;
4   a controller, coupled to the sequence of at least one codec,
5 adapted to controlling communications between the processor and the
6 sequence of at least one codec;
7   the sequence of at least one codec, each codec comprising:
8   a port coupled to the processor and the controller; and
9   a semiconductor device for distributed device identifier
10 number assignment and device counting coupled to the port.

1 24. (Original) The system of claim 23, wherein the semiconductor
2 device further comprising:

3   a counter, coupled to an input/output node, the counter for
4   counting a number of pulses in a sequence of pulses received at the
5   input/output node;

6   a first storage location to store a first count result; and

7   a pulse generator, for generating a specified length sequence
8   of pulses, the specified length being one less than the number of
9   pulses in the sequence of pulses received at the input/output node.

1   25. (Original) The system of claim 23, wherein a FSD signal line
2   of a final codec in the sequence of at least one codec is connected
3   to an external pulse generator.

1   26. (Original) The system of claim 23, wherein the semiconductor
2   device operates each time the system is reset.

1   27. (Original) The system of claim 23, wherein the semiconductor
2   device operates each time the system is powered-up.

28 to 47. (Canceled)